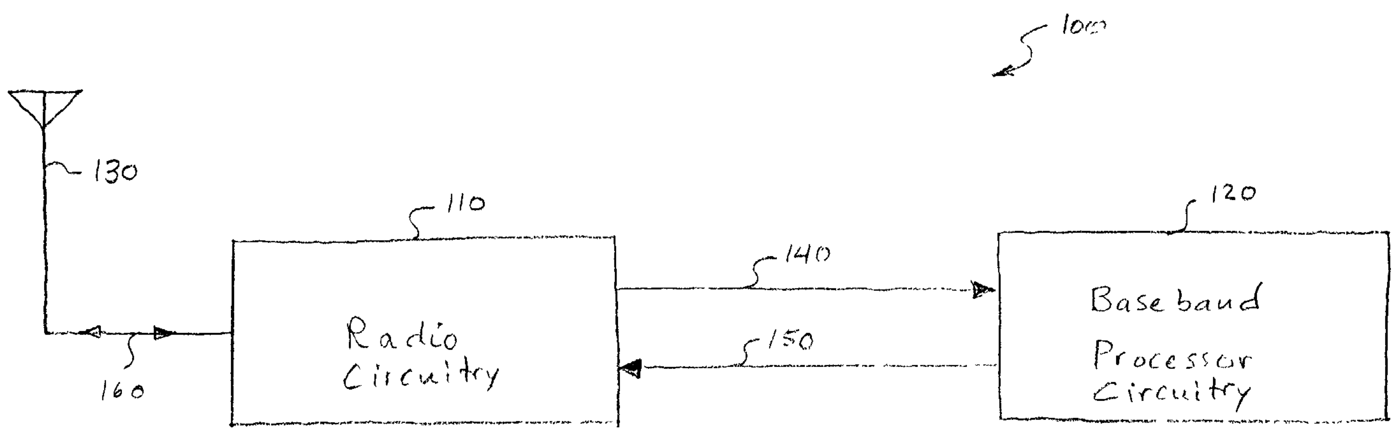

100
130
110
120
140
150
160
Radio Circuitry
Baseband Processor Circuitry

FIG. 1

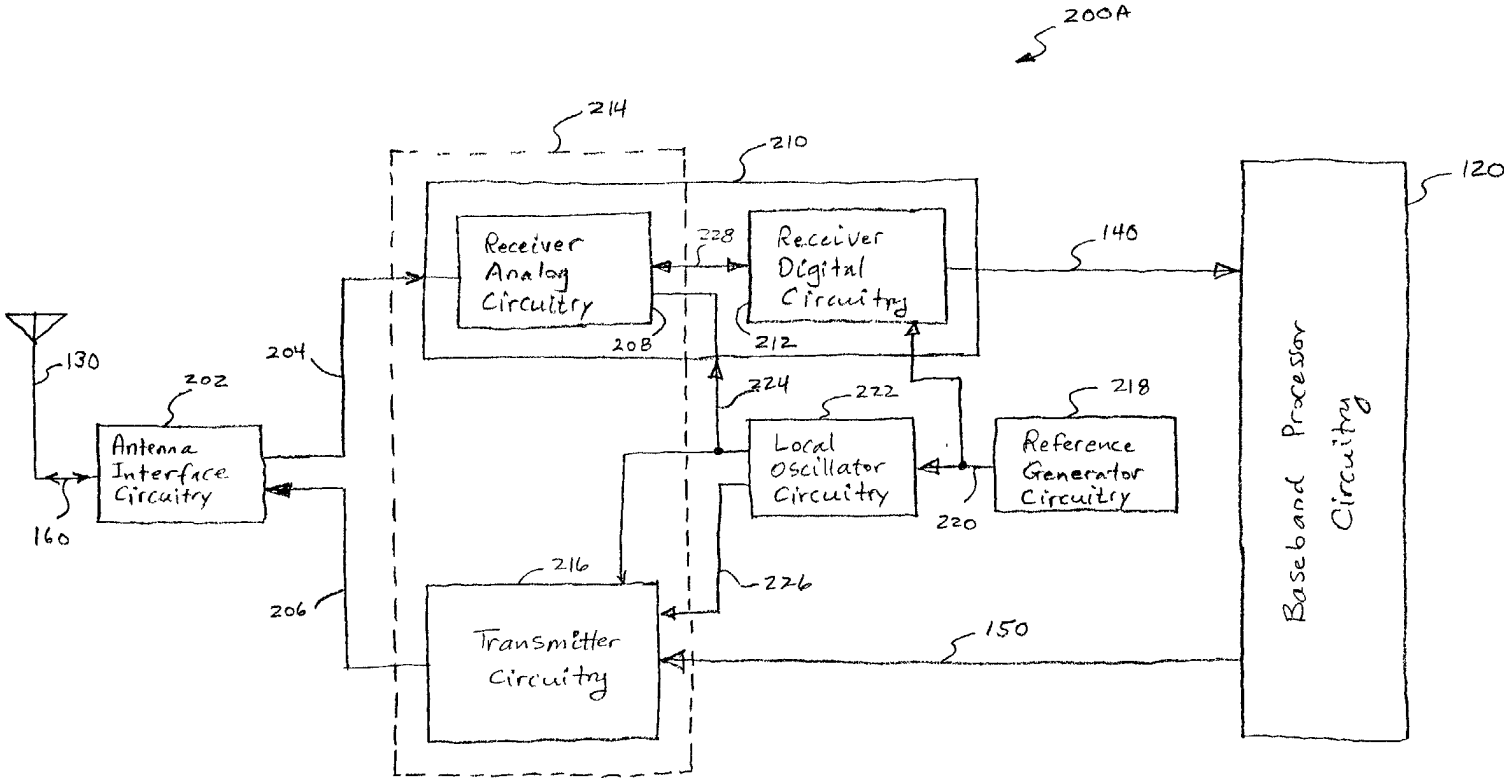


FIG. 2A

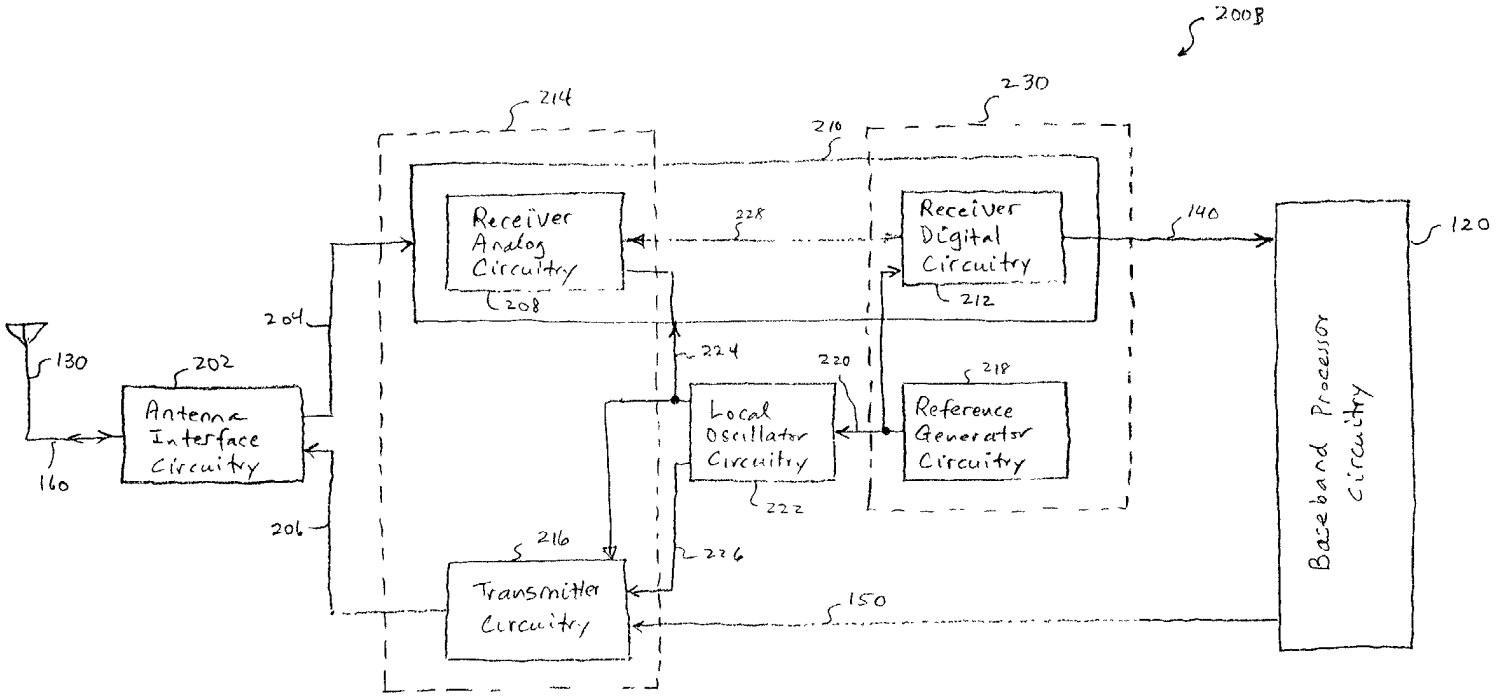


FIG. 2B

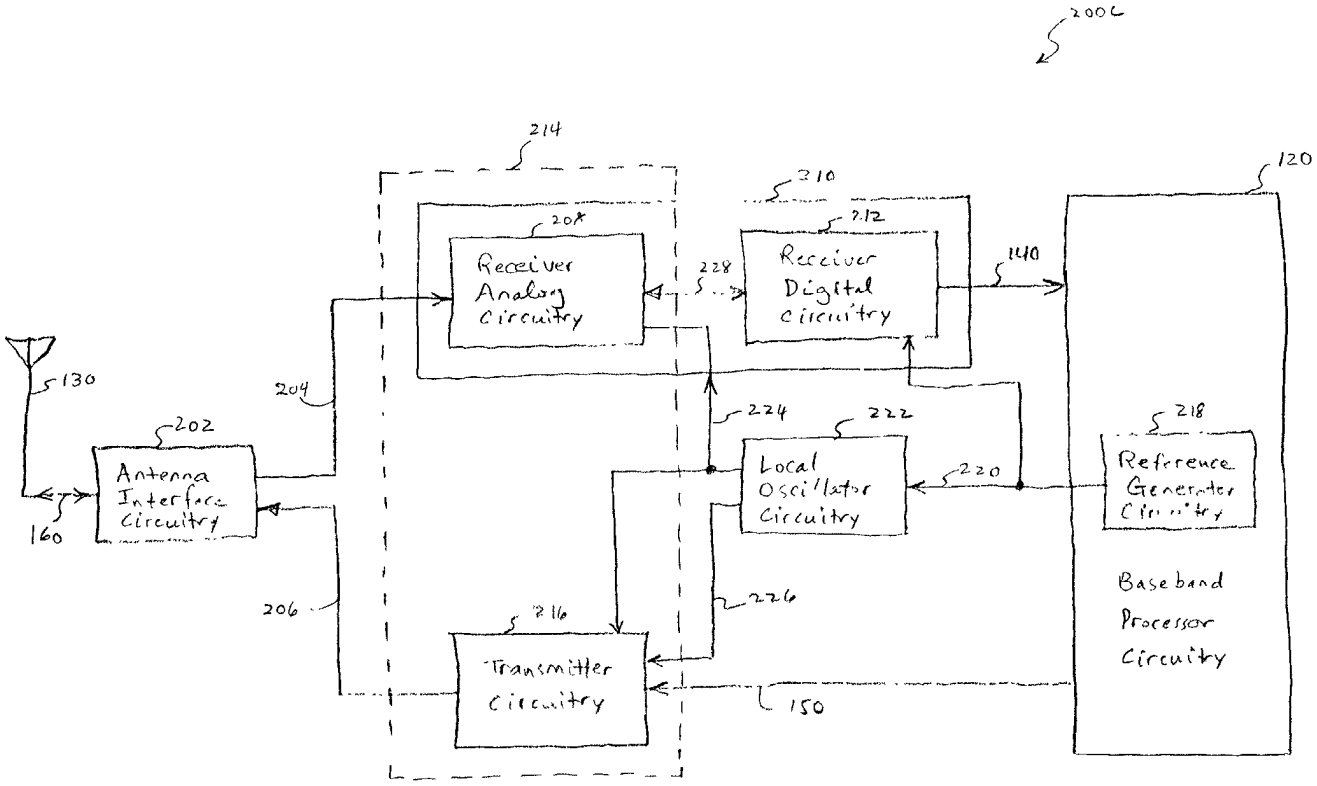


FIG. 2C

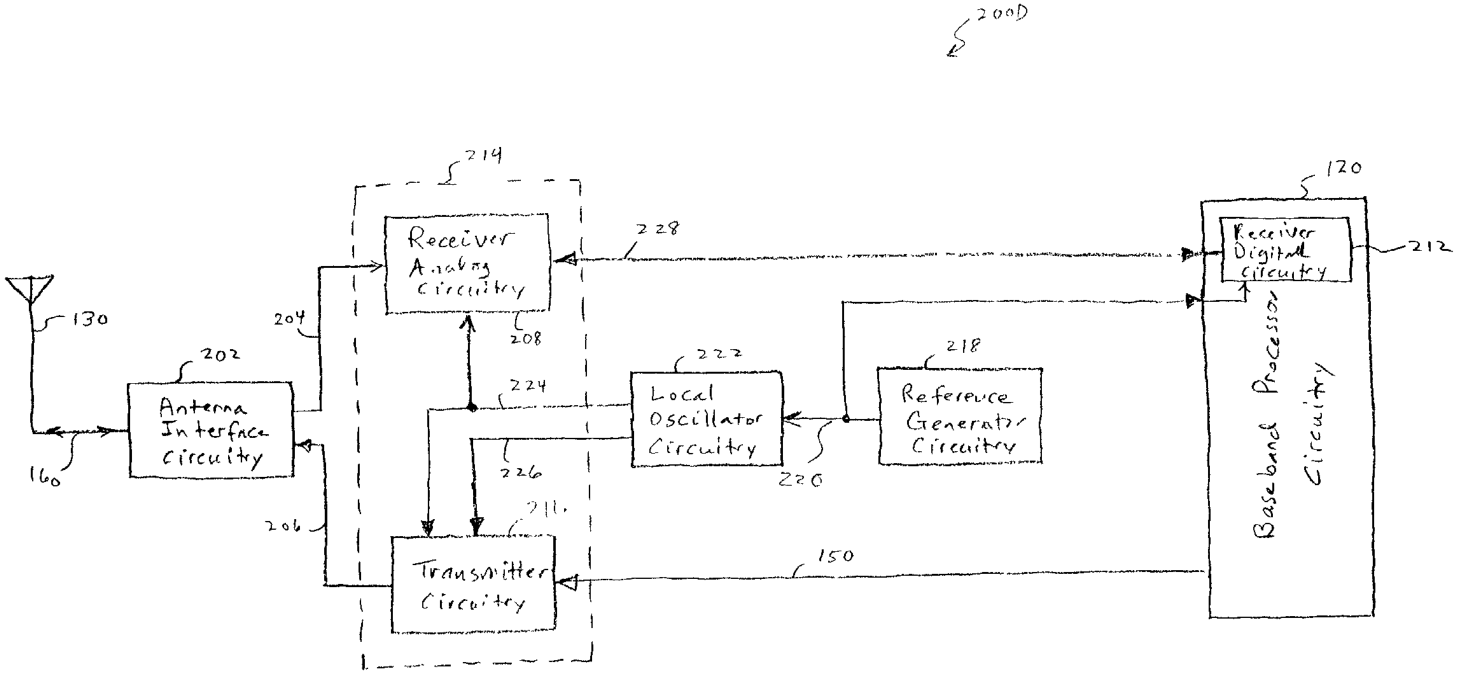

200D
214
120
Receiver Analog Circuitry
228
Receiver Digital Circuitry
212
130
204
208
202
224
222
218
Antenna Interface Circuitry
Local Oscillator Circuitry
Reference Generator Circuitry
Baseband Processor Circuitry
160
226
220
206
211
150
Transmitter Circuitry

FIG. 2D

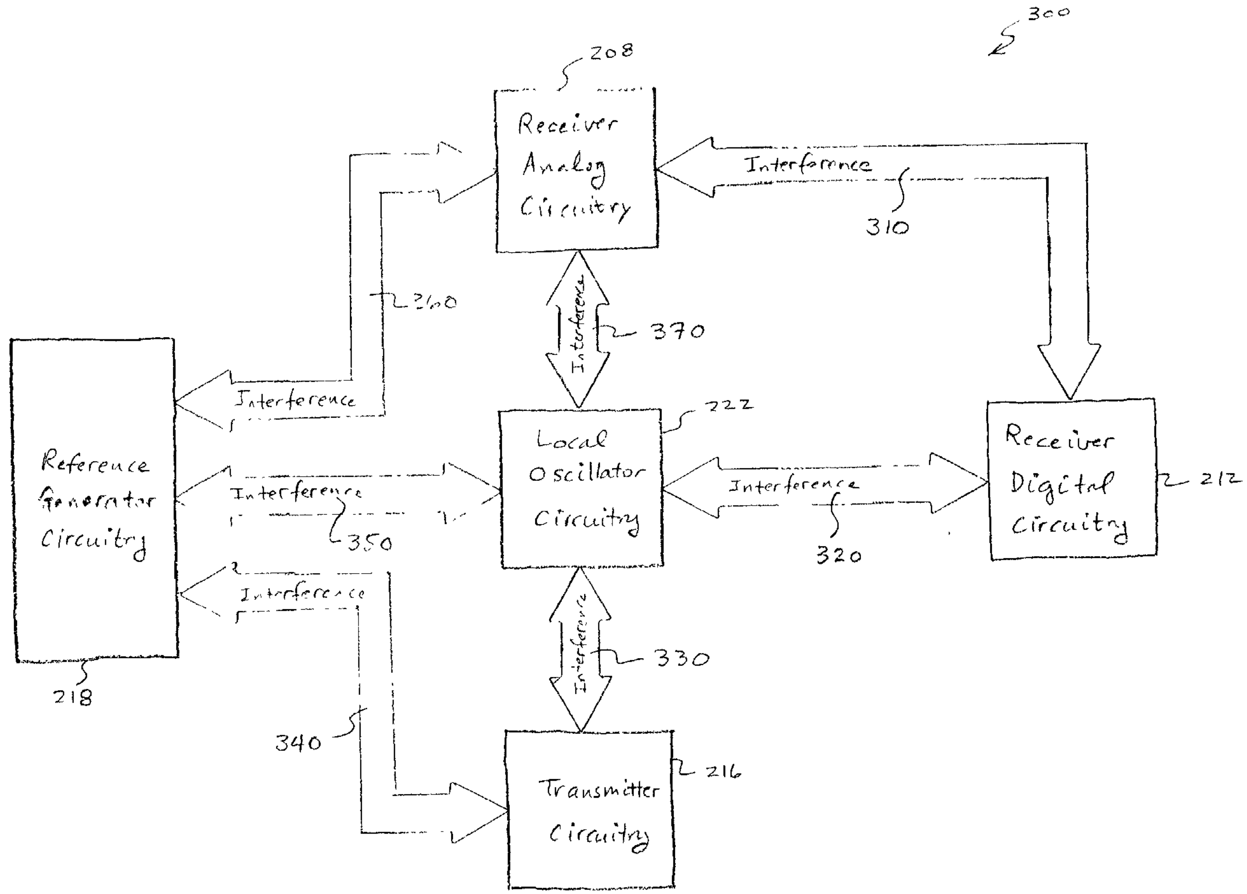

300
208
Receiver Analog Circuitry
Interference
310
Receiver Digital Circuitry
212
Interference
370
Local Oscillator Circuitry
222
Interference
320
Interference
330
Transmitter Circuitry
216
Reference Generator Circuitry
218
Interference
360
Interference
350
Interference
340

FIG. 3

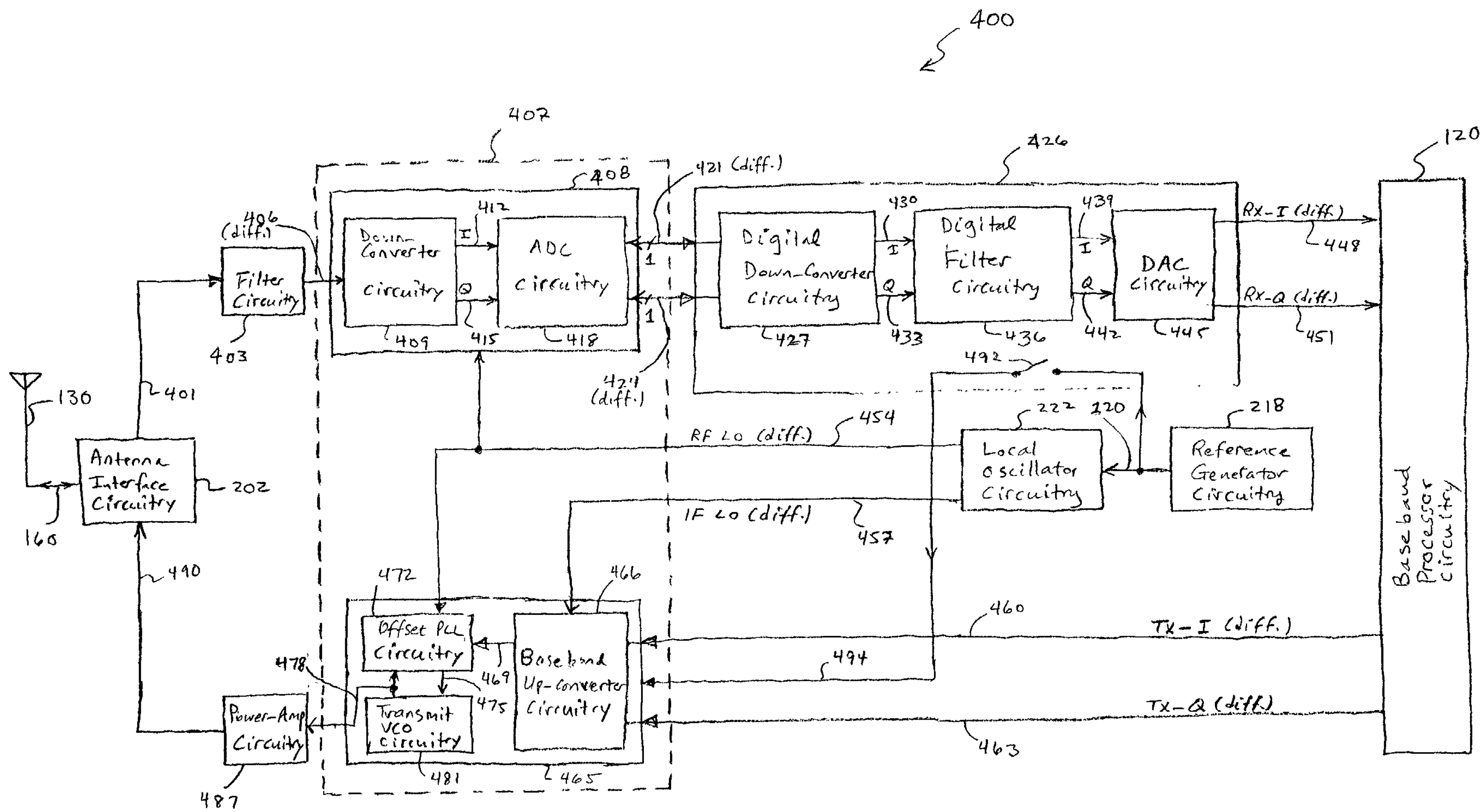

400
407
408
426
120
421 (diff.)
406 (diff.)
Filter Circuitry
403
Down-Converter circuitry
409
412
I
Q
415
ADC circuitry
418
1
1
424 (diff.)
Digital Down-Converter circuitry
427
430
433
Digital Filter Circuitry
436
439
442
DAC circuitry
445
Rx-I (diff.)
448
Rx-Q (diff.)
451
Baseband Processor circuitry
130
401
Antenna Interface Circuitry
202
160
490
492
222
120
218
Local Oscillator Circuitry
Reference Generator Circuitry
RF LO (diff.)
454
IF LO (diff.)
457
472
466
Offset PLL Circuitry
Baseband Up-Converter Circuitry
469
475
Transmit VCO circuitry
481
465
478
Power-Amp Circuitry
487
460
Tx-I (diff.)
494
Tx-Q (diff.)
463

FIG. 4

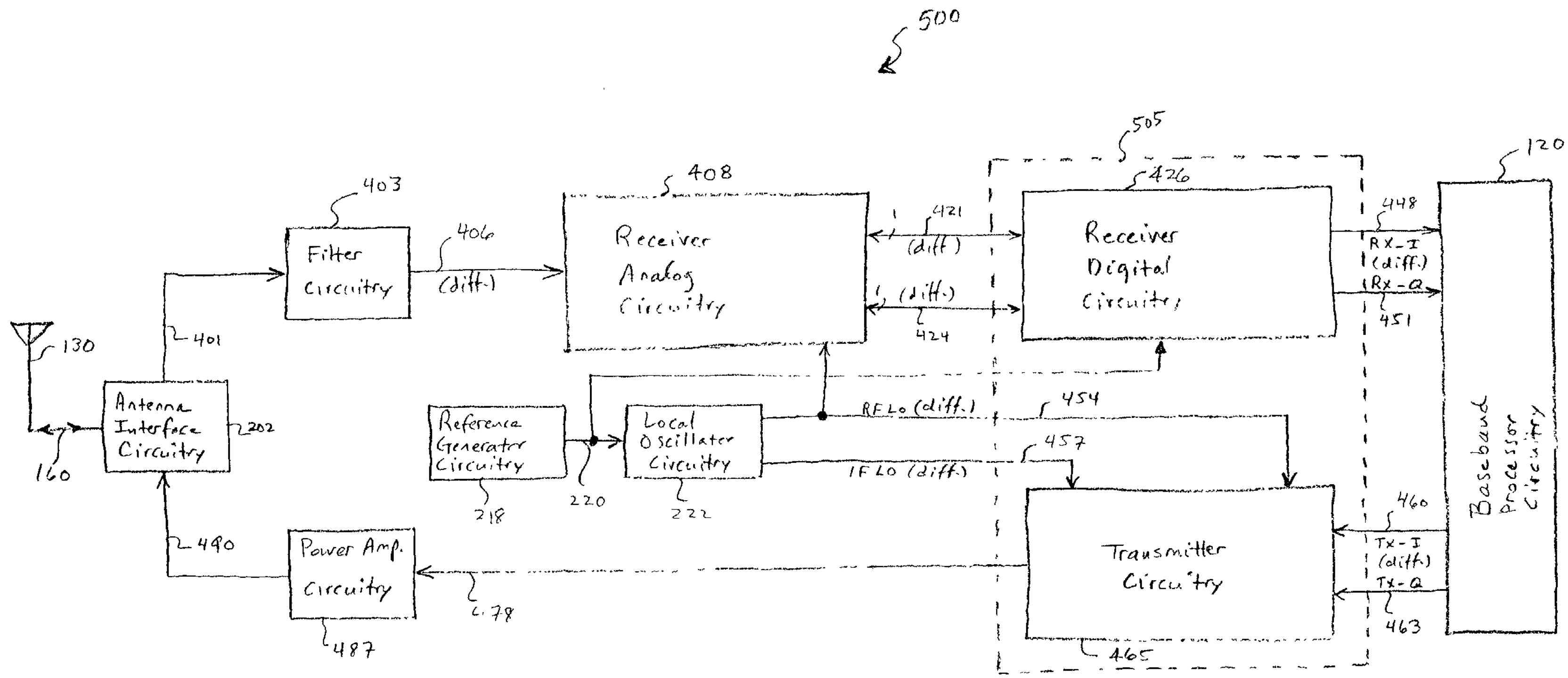

500
505
120
408
403
426
Antenna Interface Circuitry
Filter Circuitry
Receiver Analog Circuitry
Receiver Digital Circuitry
Baseband Processor Circuitry
Reference Generator Circuitry
Local Oscillator Circuitry
Transmitter Circuitry
Power Amp. Circuitry
130
160
202
401
406
(diff.)
421
(diff.)
(diff.)
424
448
RX-I
(diff.)
RX-Q
451
RF LO (diff.)
454
457
IF LO (diff.)
218
220
222
460
TX-I
(diff.)
TX-Q
463
465
490
478
487

FIG. 5

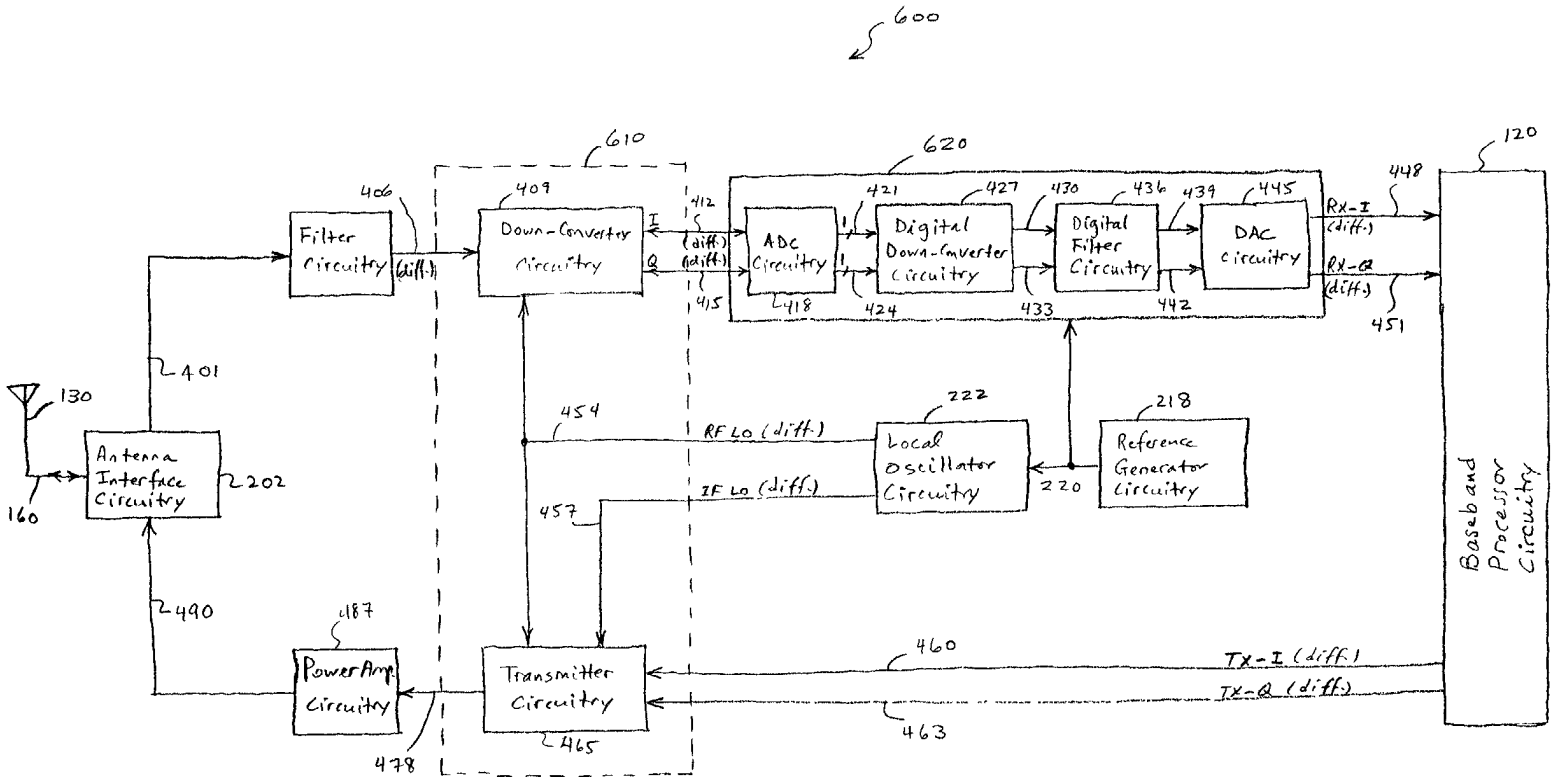

600
610
620
120
406
409
412
421
427
430
436
439
445
448
Filter Circuitry
Down-Converter Circuitry
I
Q
(diff.)
ADC Circuitry
Digital Down-Converter Circuitry
Digital Filter Circuitry
DAC circuitry
Rx-I (diff.)
Rx-Q (diff.)
415
418
424
433
442
451
401
130
160
Antenna Interface Circuitry
202
454
RF LO (diff.)
222
Local Oscillator Circuitry
218
Reference Generator Circuitry
220
IF LO (diff.)
457
Baseband Processor Circuitry
490
187
PowerAmp Circuitry
Transmitter Circuitry
460
Tx-I (diff.)
Tx-Q (diff.)
463
465
478

FIG. 6

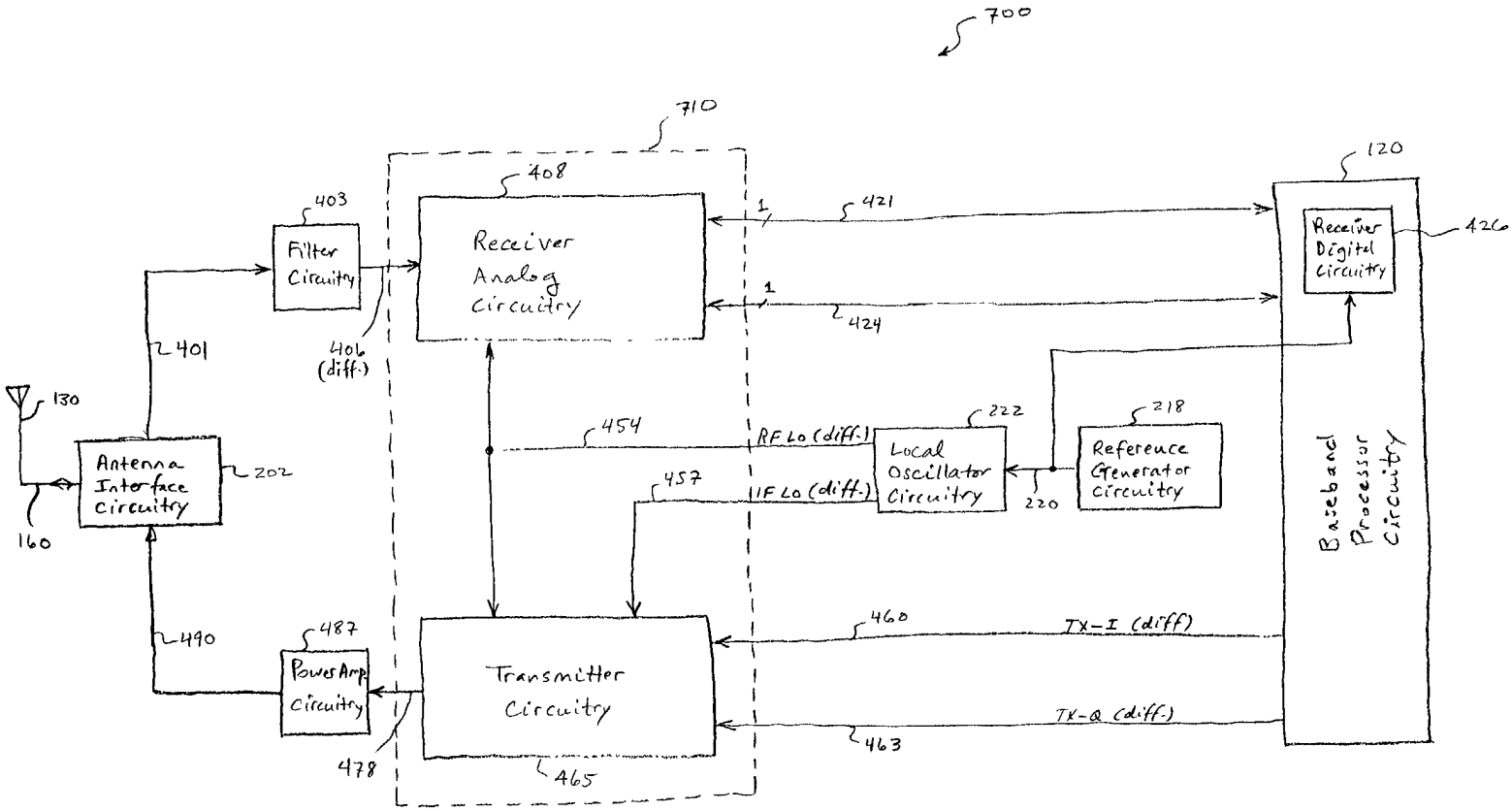

700
710
408
403
Filter Circuitry
Receiver Analog Circuitry
1
421
120
Receiver Digital Circuitry
426
1
424
406 (diff.)
401
130
454
RF LO (diff.)
222
Local Oscillator Circuitry
218
Reference Generator Circuitry
220
457
IF LO (diff.)
Antenna Interface Circuitry
202
160
Baseband Processor Circuitry
460
TX-I (diff)
490
487
Power Amp Circuitry
Transmitter Circuitry
TX-Q (diff.)
463
478
465

FIG. 7

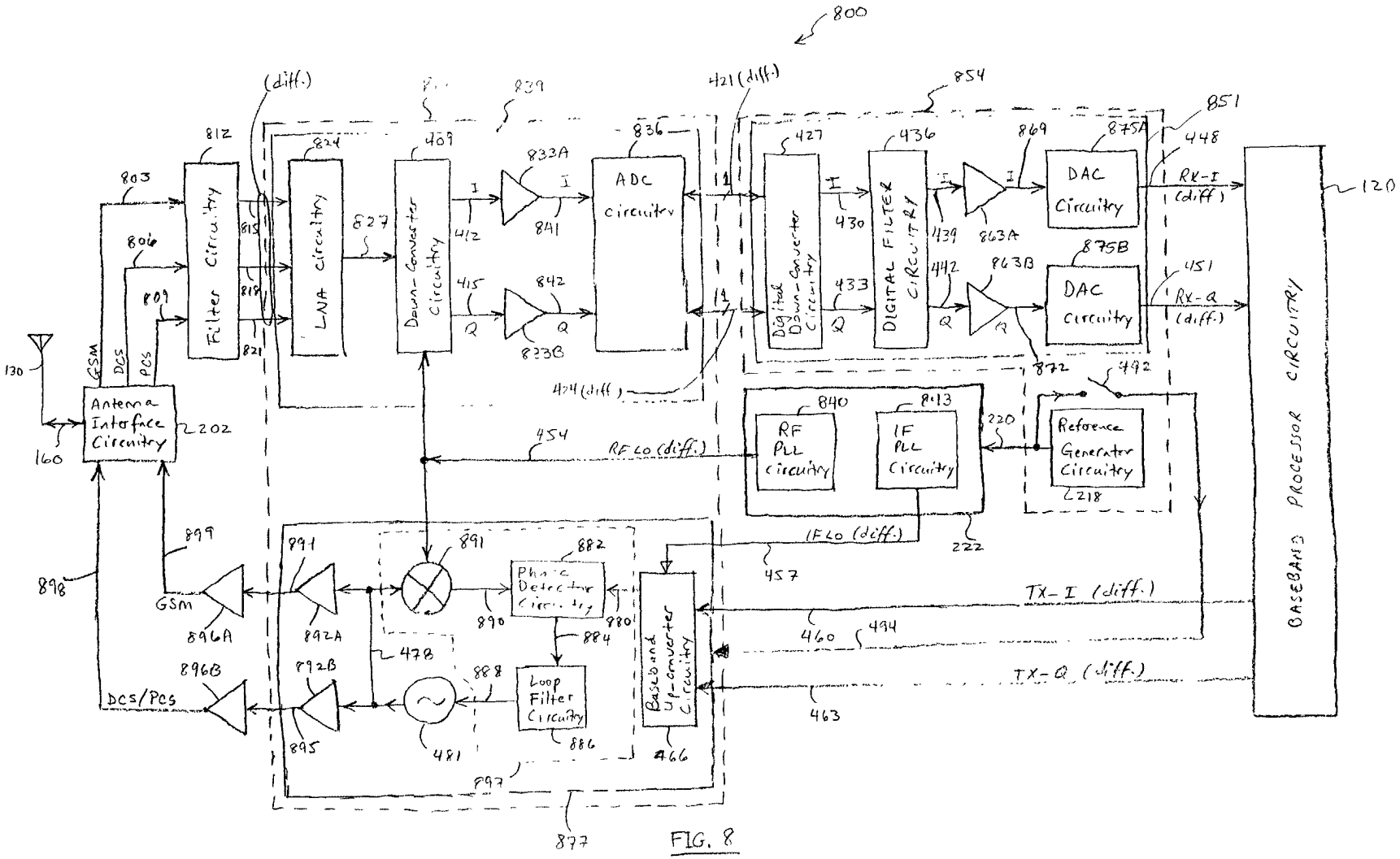


FIG. 8

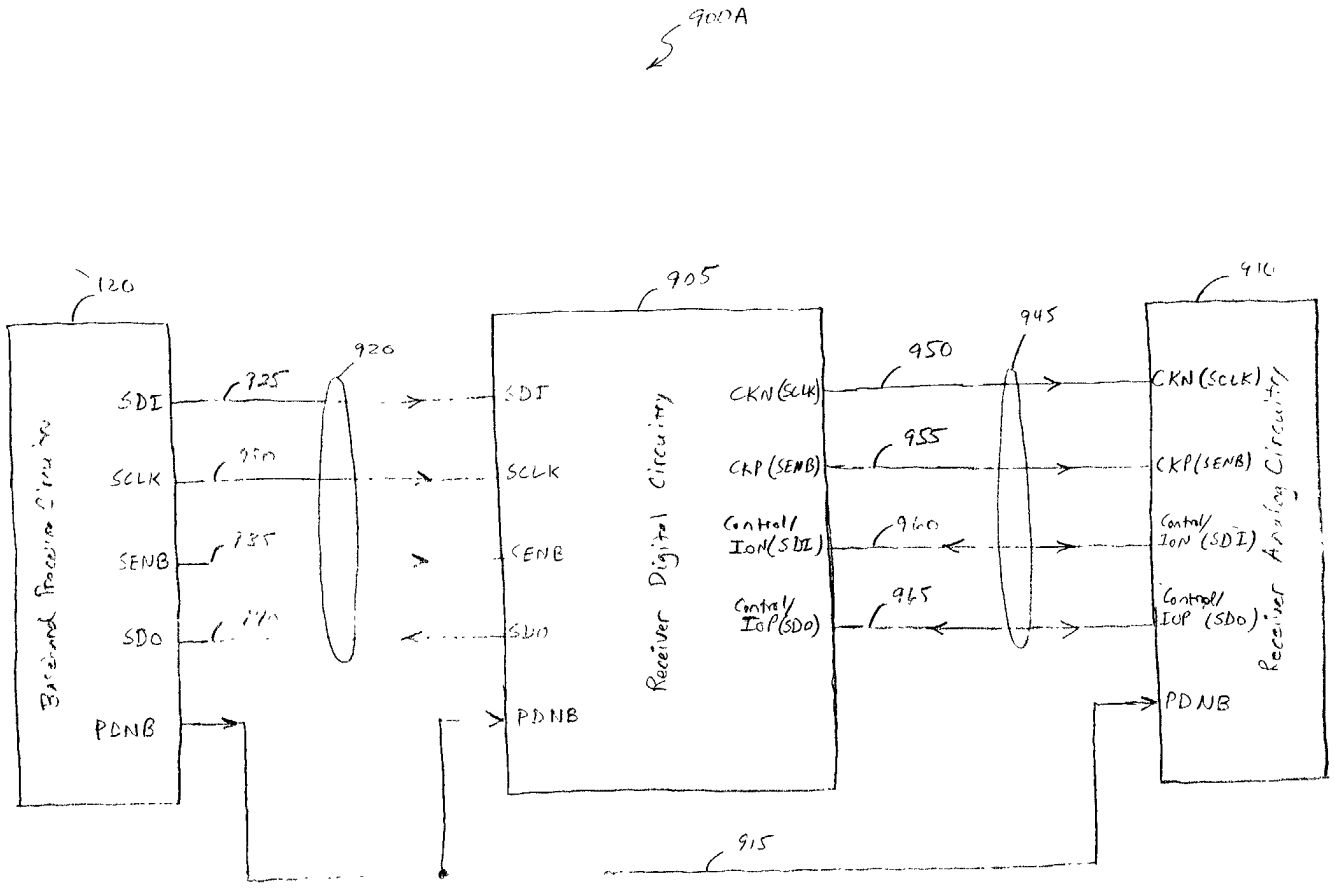
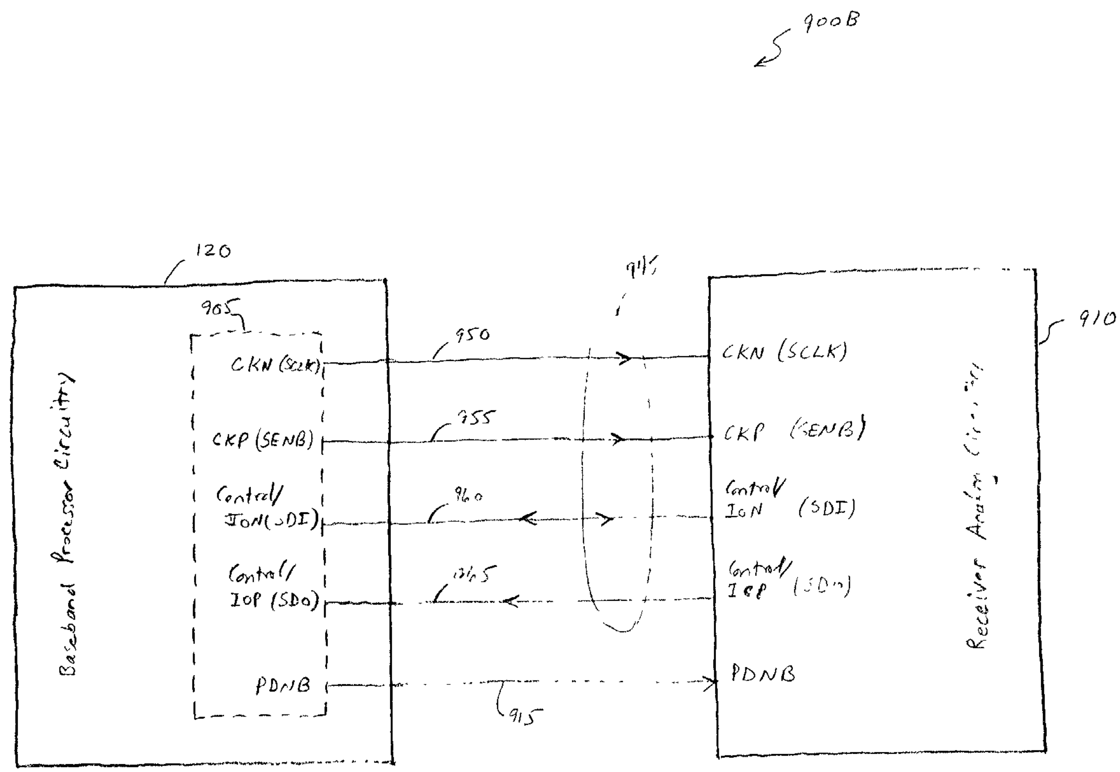

900A
120
905
910
945
920
950
925
955
930
960
935
965
940
SDI
SCLK
SENB
SDO
PDNB
Backend Processing Circuitry
SDI
SCLK
SENB
SDO
PDNB
Receiver Digital Circuitry
CKN (SCLK)
CKP (SENB)
Control IoN (SDI)
Control IoP (SDO)
CKN (SCLK)
CKP (SENB)
Control IoN (SDI)
Control IoP (SDO)
PDNB
Receiver Analog Circuitry
915

FIG. 9A



900B
120
905
Baseband Processor Circuitry
CKN (SCLK)
CKP (SENB)
Control/ ION (SDI)
Control/ IOP (SDO)
PDNB
950
955
960
965
915
910
Receiver Analog Circuitry
CKN (SCLK)
CKP (SENB)
Control/ ION (SDI)
PDNB

FIG. 9B

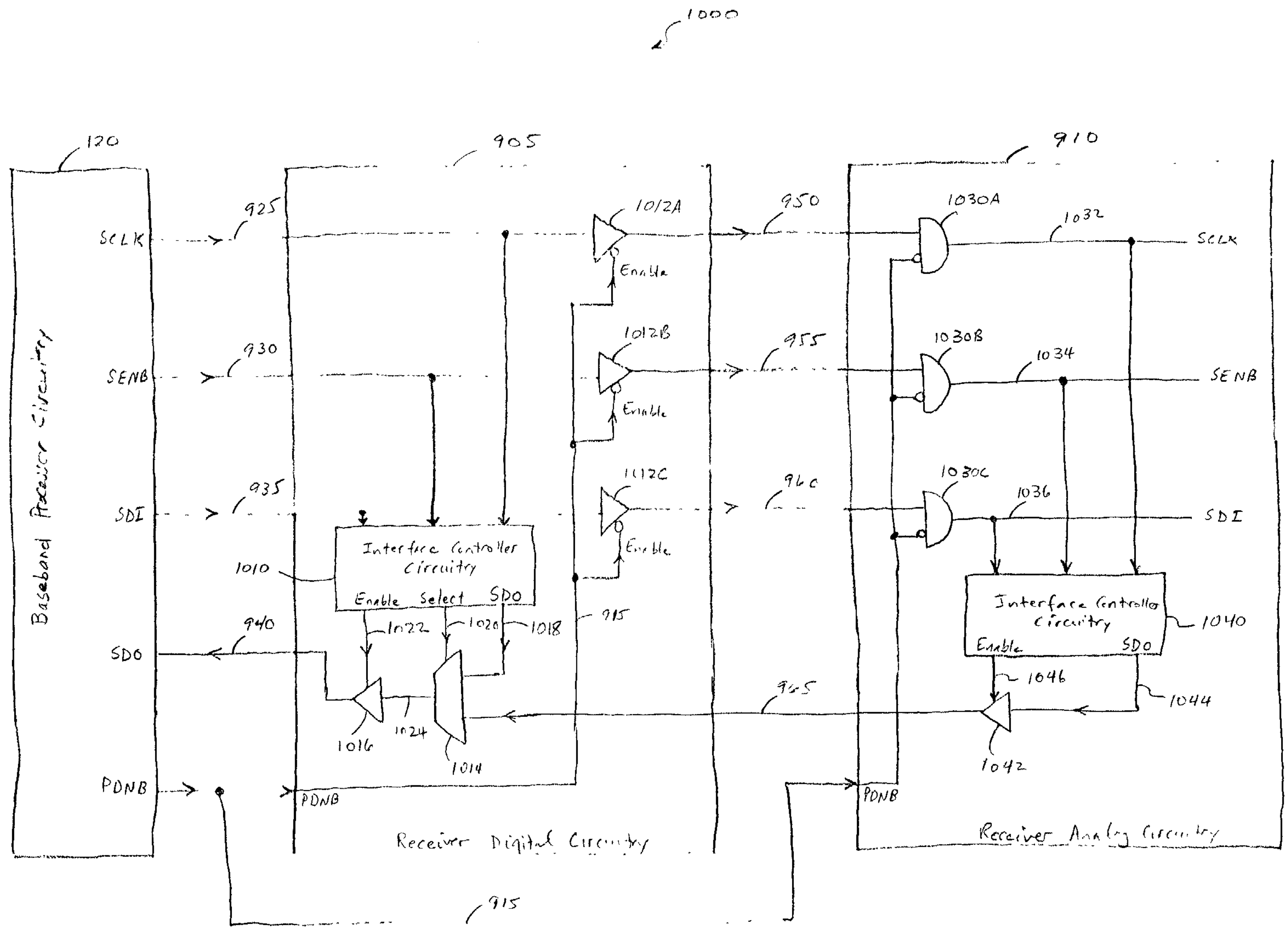

1000
120
905
910
Baseband Processor Circuitry
SCLK
SENB
SDI
SDO
PDNB
925
930
935
940
Interface Controller Circuitry
Enable
Select
SDO
1010
1022
1020
1018
1024
1016
1014
PDNB
915
Receiver Digital Circuitry
1012A
1012B
1112C
Enable
950
955
960
965
1030A
1030B
1030C
1032
1034
1036
Interface Controller Circuitry
Enable
SDO
1040
1046
1044
1042
PDNB
Receiver Analog Circuitry

FIG. 10

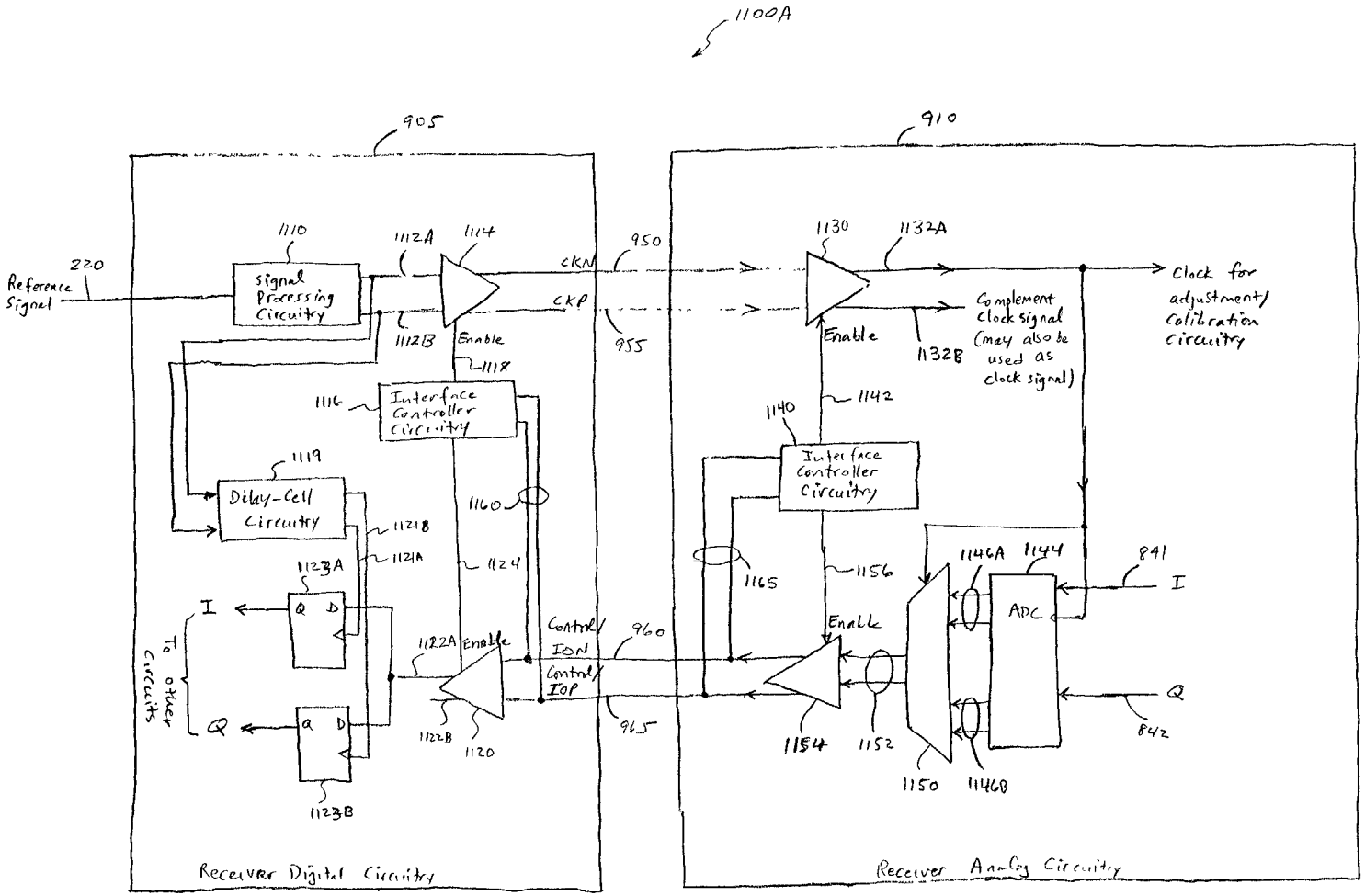

1100A
905
910
1110
1112A
1114
220
Reference Signal
Signal Processing Circuitry
950
CKN
CKP
955
1130
1132A
Clock for adjustment/ calibration circuitry
Complement Clock signal (may also be used as clock signal)
1132B
Enable
1112B
Enable
1118
1116
Interface Controller Circuitry
1142
1140
Interface Controller Circuitry
1119
Delay-Cell Circuitry
1160
1121B
1121A
1124
1123A
1165
1156
1146A
1144
841
I
ADC
Q
D
I
To other circuits
1122A
Enable
Control ION
Control IOP
960
Enable
Q
D
Q
842
1122B
1120
965
1154
1152
1150
1146B
1123B
Receiver Digital Circuitry
Receiver Analog Circuitry

FIG. 11A

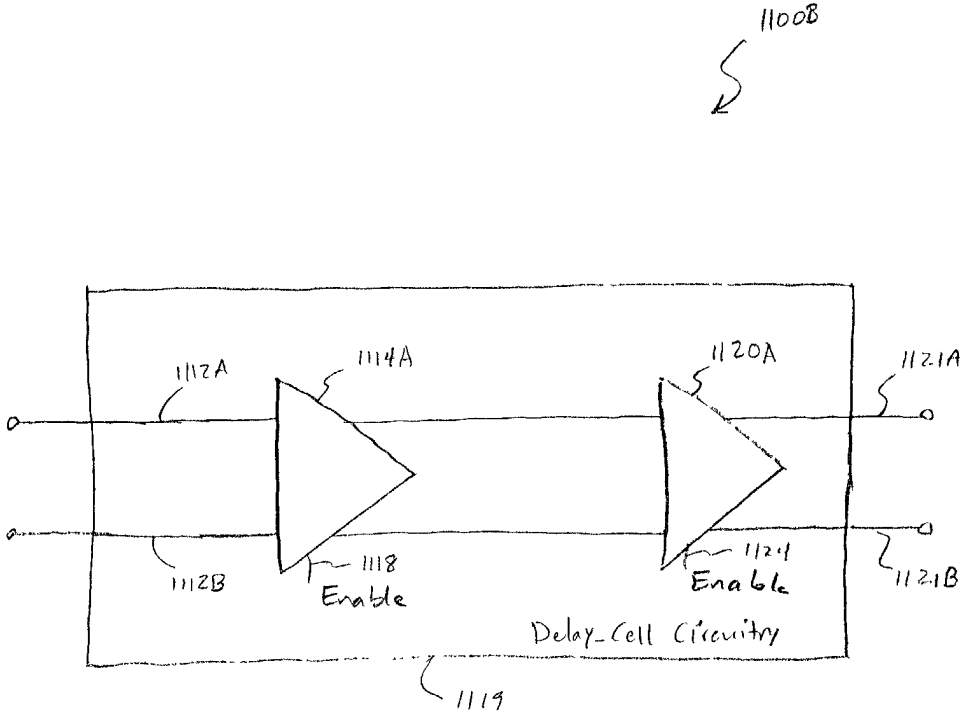


FIG. 11B

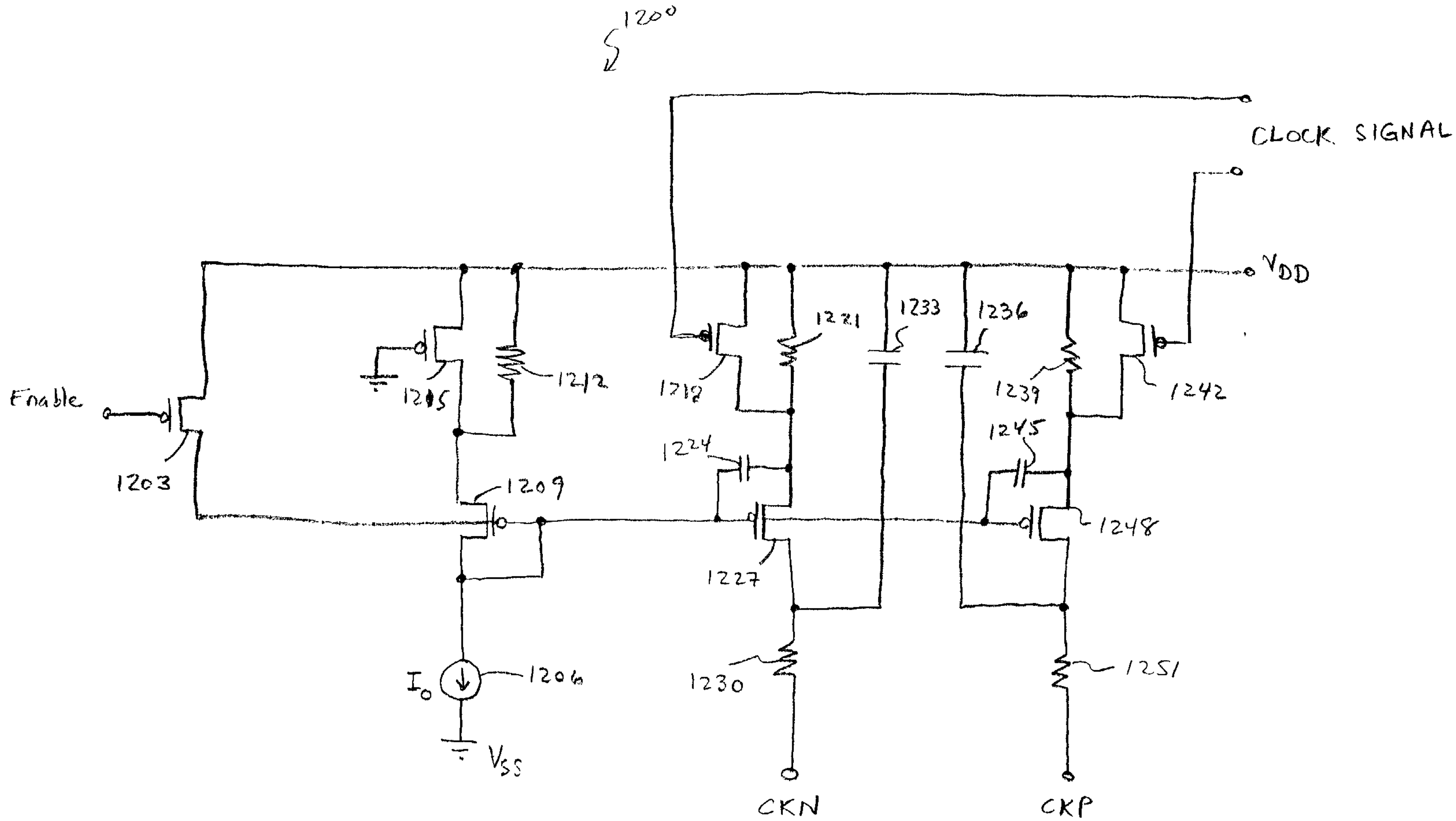

1200
CLOCK SIGNAL
V_{DD}
Enable
1203
1215
1212
1209
I_o
1206
V_{SS}
1218
1221
1224
1227
1230
1233
1236
1239
1242
1245
1248
1251
CKN
CKP

FIG. 12

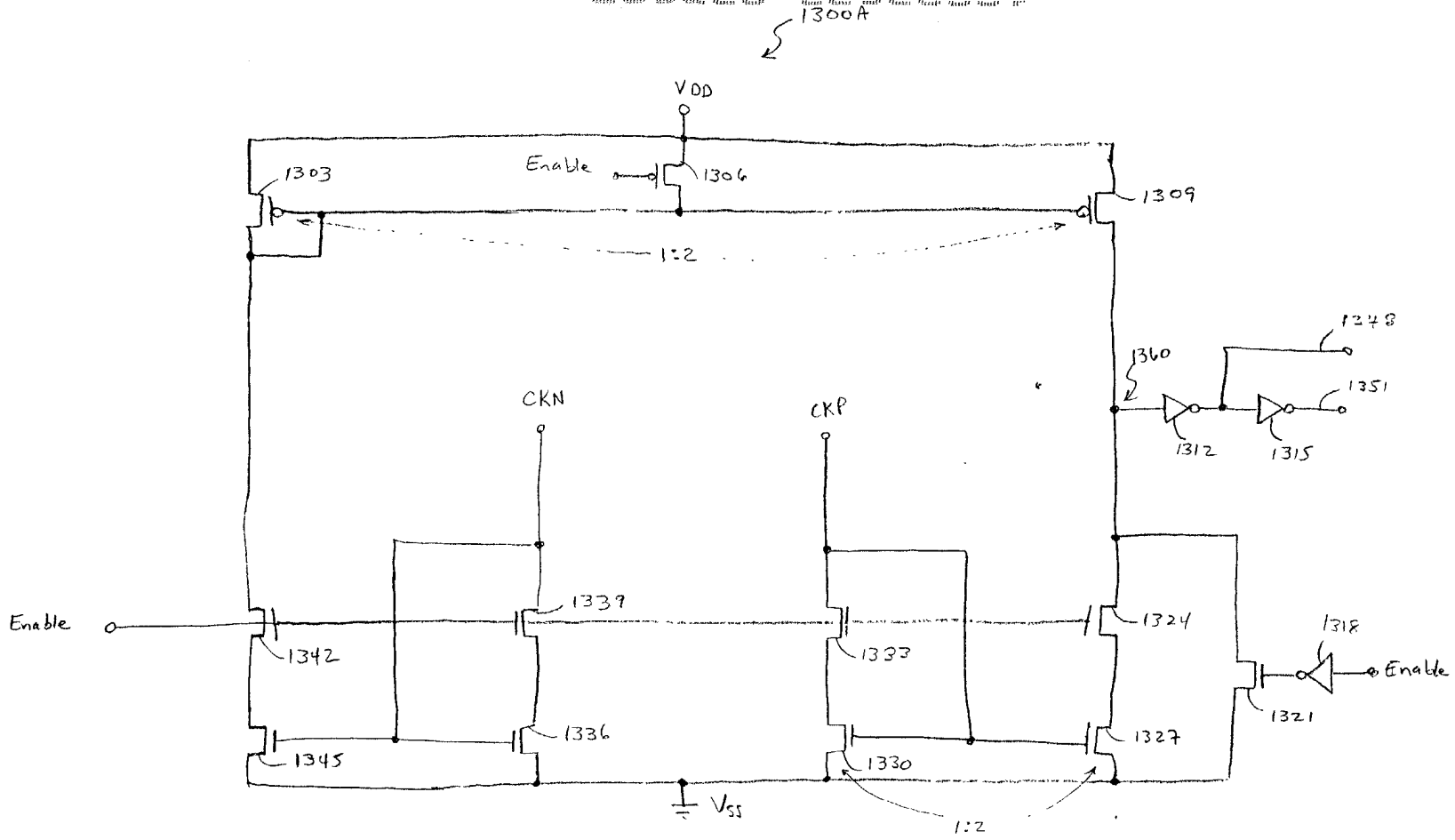
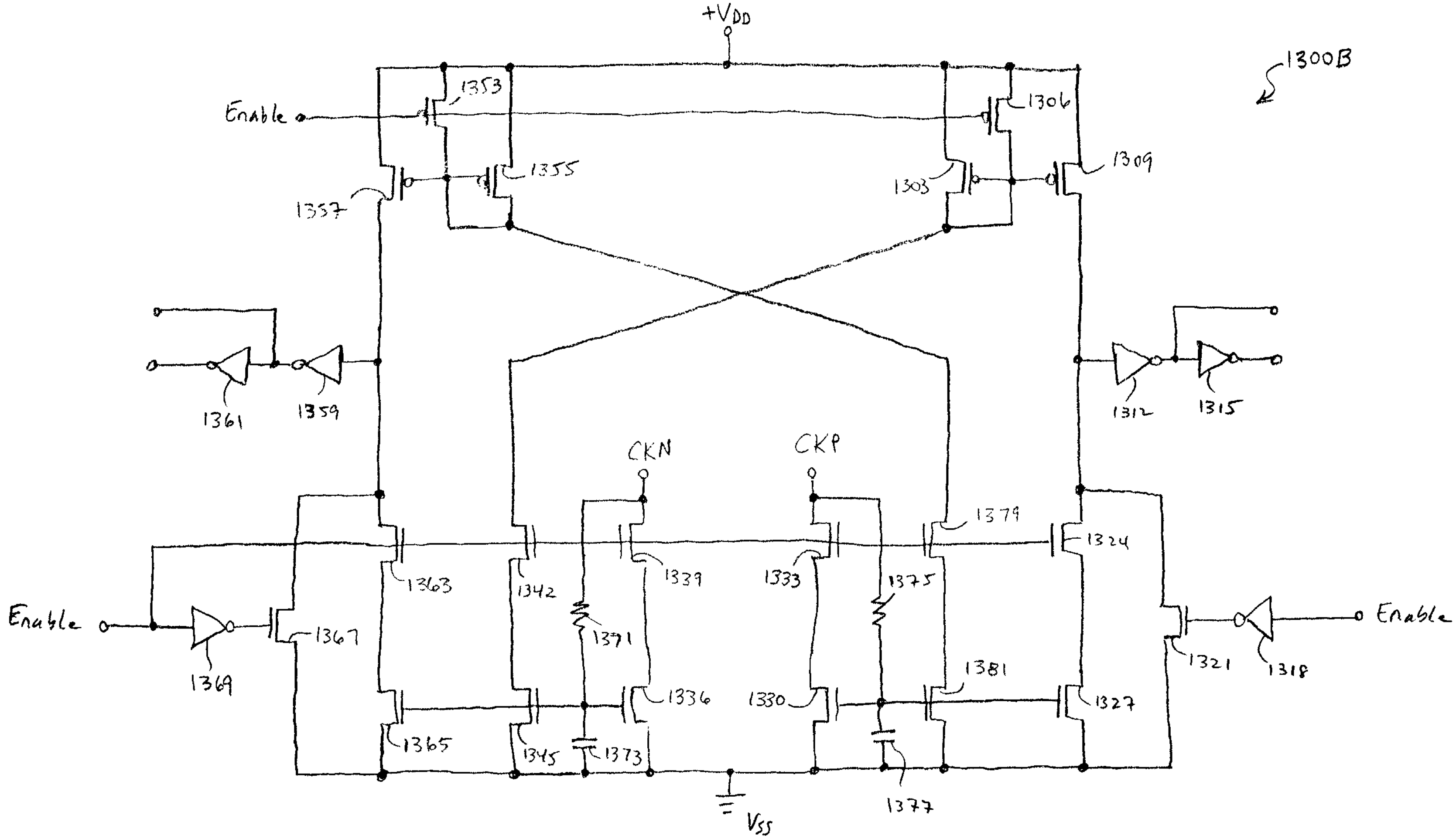

1300A
VDD
1303
Enable
1306
1309
1:2
1348
1360
1351
CKN
CKP
1312
1315
Enable
1339
1342
1333
1324
1318
Enable
1321
1336
1345
1327
1330
Vss
1:2

FIG. 13A



+VDD
1300B
Enable
1353
1306
1355
1303
1309
1357
1361
1359
1312
1315
CKN
CKP
1379
1324
1363
1342
1339
1333
1375
Enable
1367
1369
1371
1321
1318
Enable
1336
1330
1381
1327
1365
1345
1373
1377
Vss

FIG. 13B

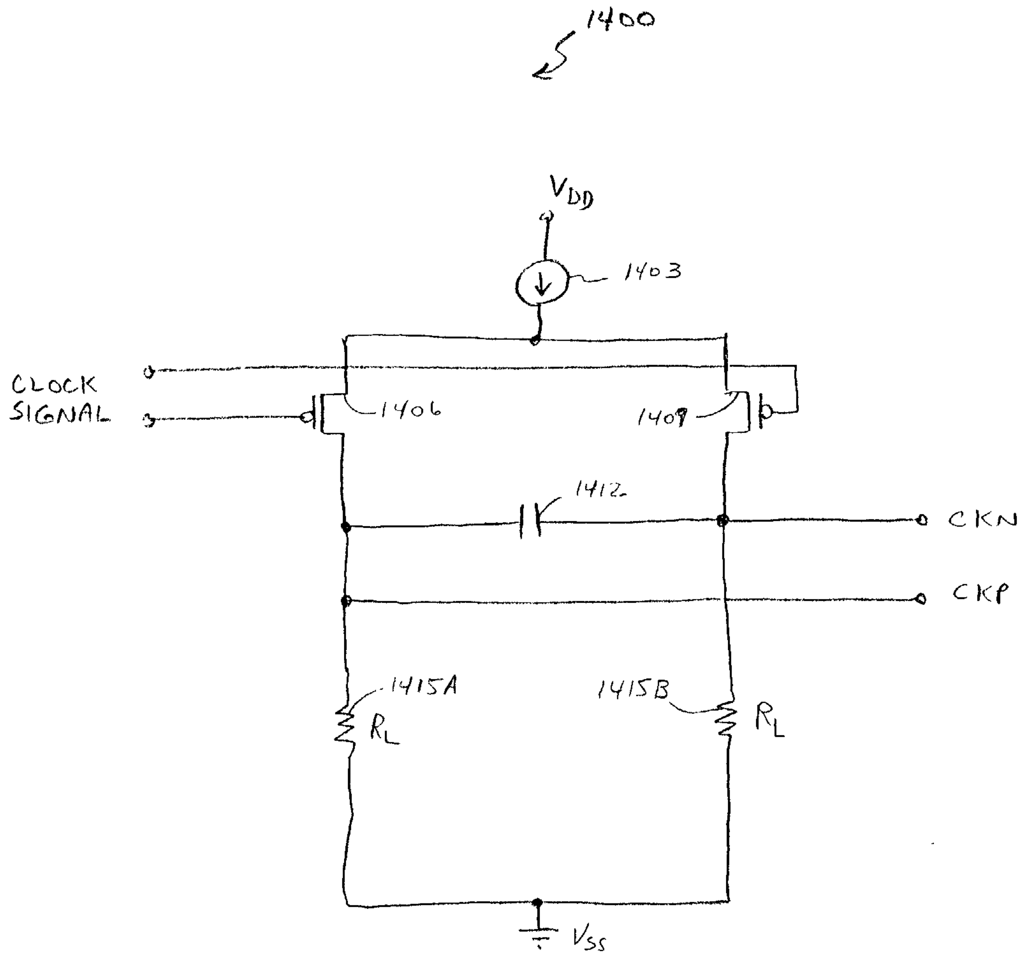

1400
VDD
1403
CLOCK
SIGNAL
1406
1409
1412
CKN
CKP
1415A
RL
1415B
RL
VSS

FIG. 14

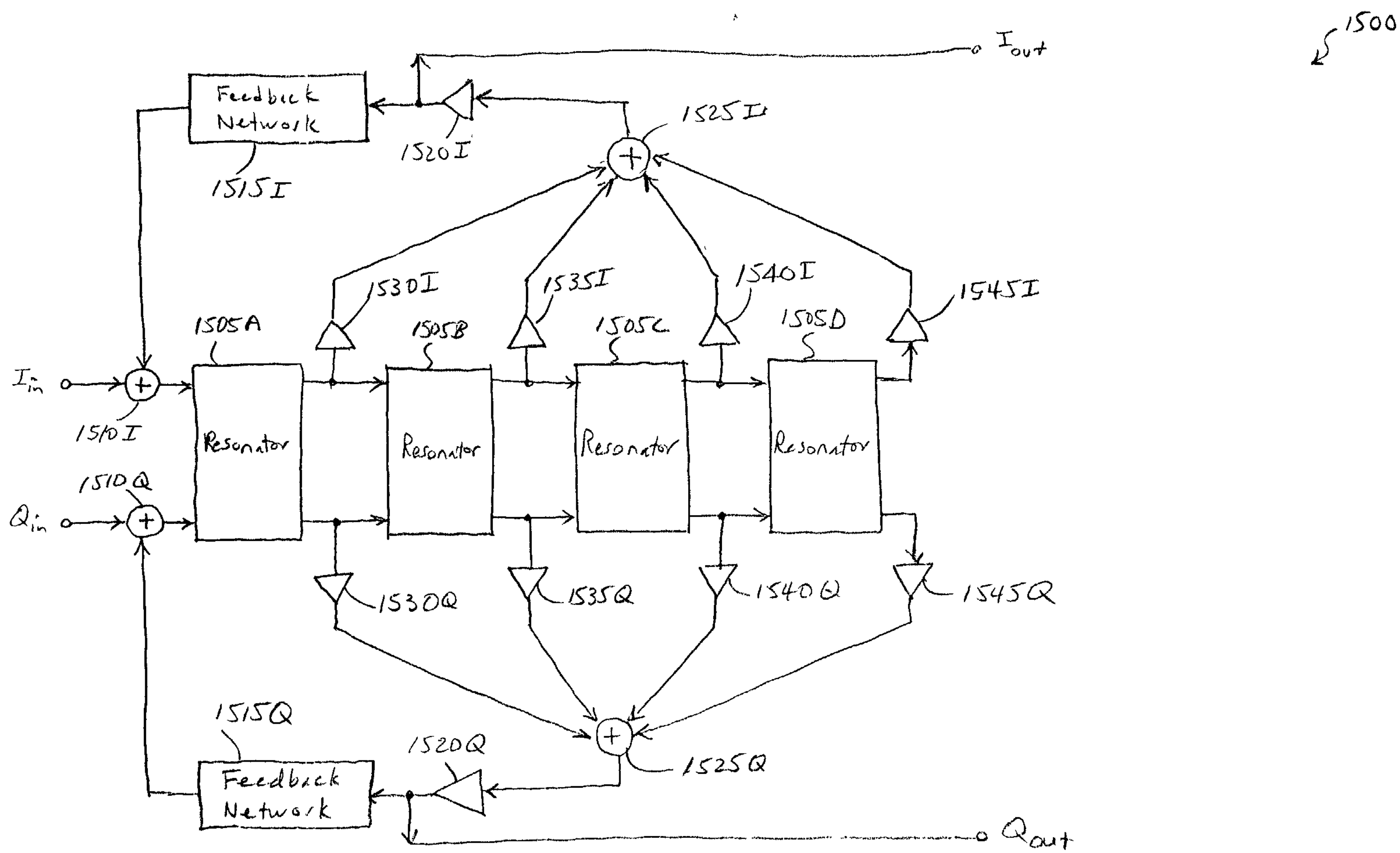

1500
Iout
Feedback Network
1515I
1520I
1525I
1530I
1535I
1540I
1545I
1505A
1505B
1505C
1505D
Iin
1510I
Resonator
Resonator
Resonator
Resonator
1510Q
Qin
1530Q
1535Q
1540Q
1545Q
1515Q
1520Q
1525Q
Feedback Network
Qout

FIG. 15

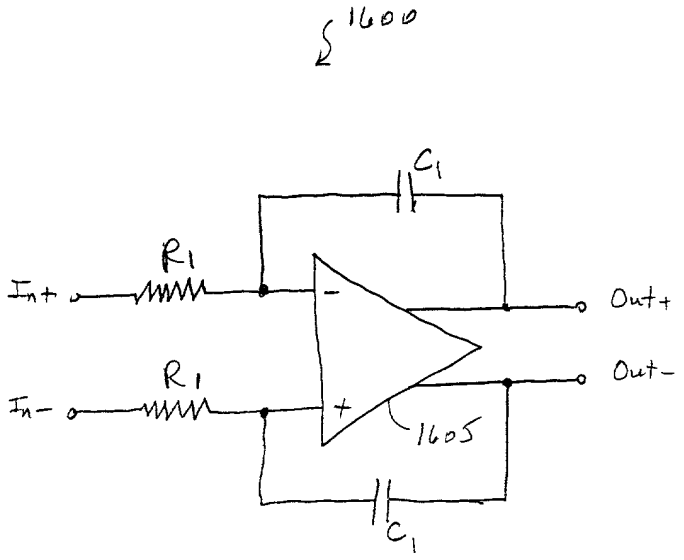

1600
C1
R1
In+
R1
In−
Out+
Out−
1605
C1

FIG. 16

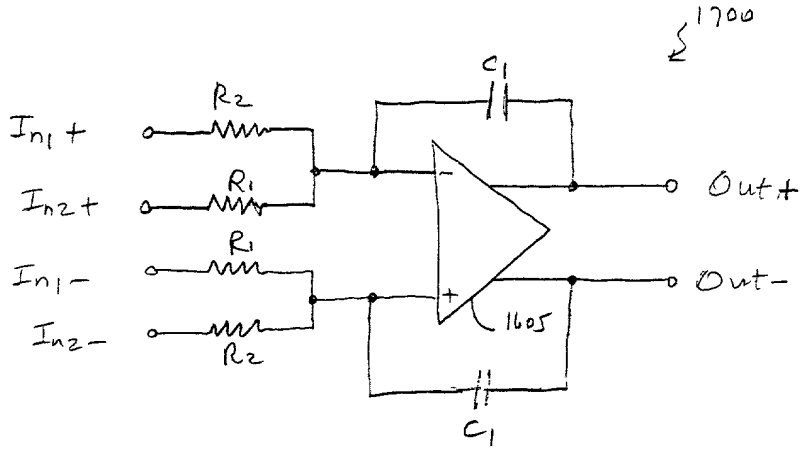

1700
C1
R2
In1+
R1
In2+
R1
In1−
In2−
R2
Out+
Out−
1605
C1

FIG. 17

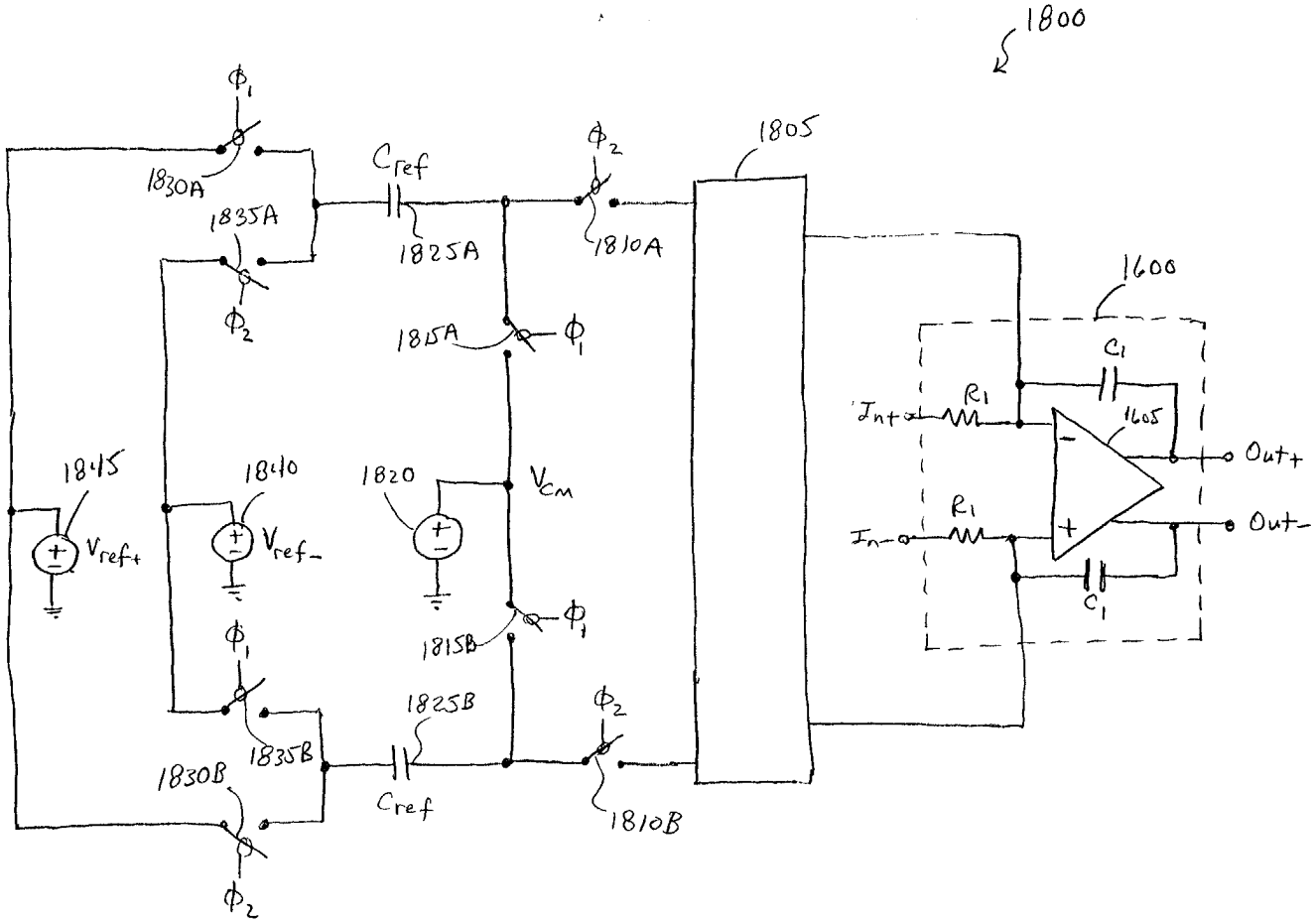
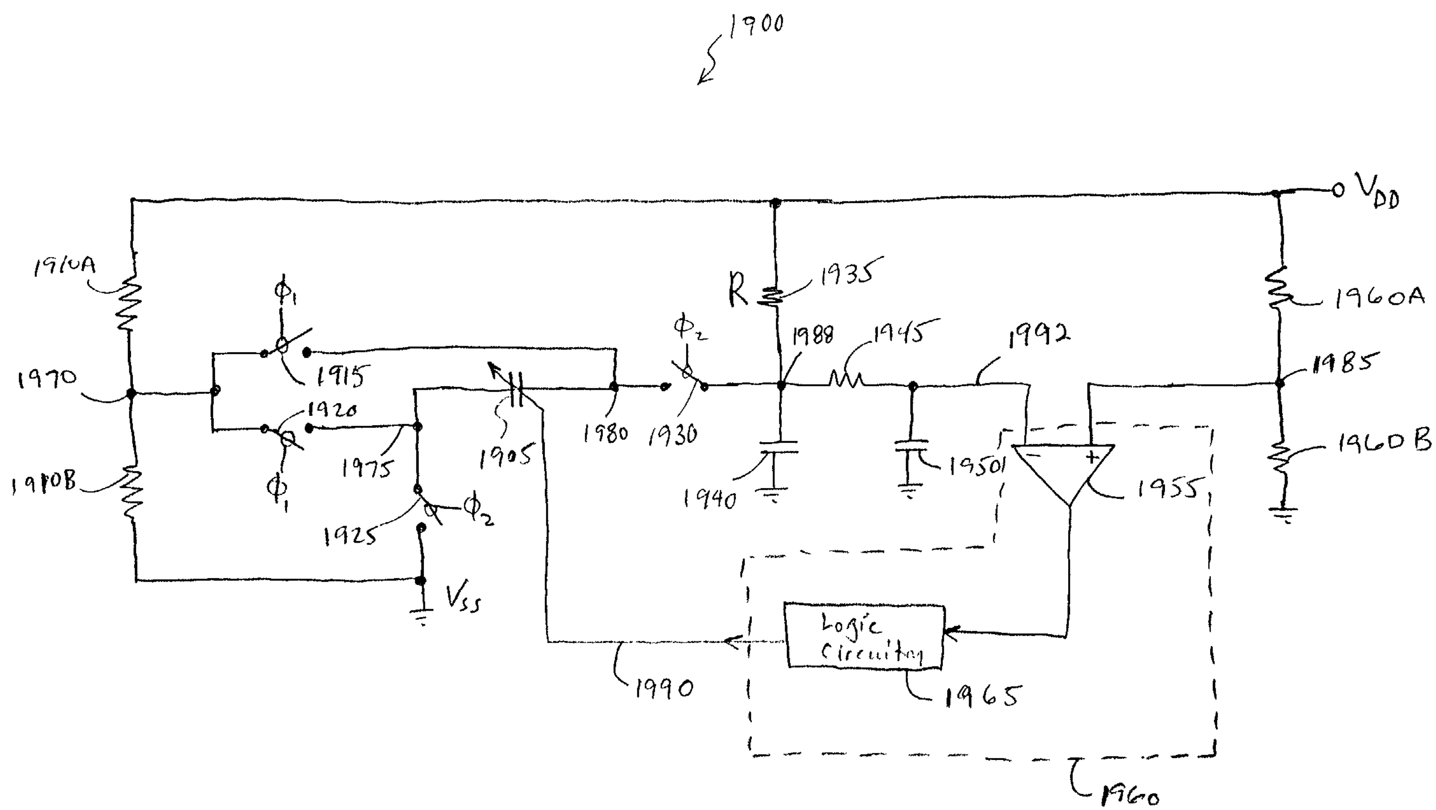


FIG. 18



1900
V_{DD}
1910A
1970
1910B
ϕ_1
1915
1920
ϕ_1
1975
1925
ϕ_2
V_{SS}
1905
1980
ϕ_2
1930
R
1935
1988
1945
1992
1940
1950
1955
1960A
1985
1960B
Logic Circuitry
1965
1990
1960

FIG. 19

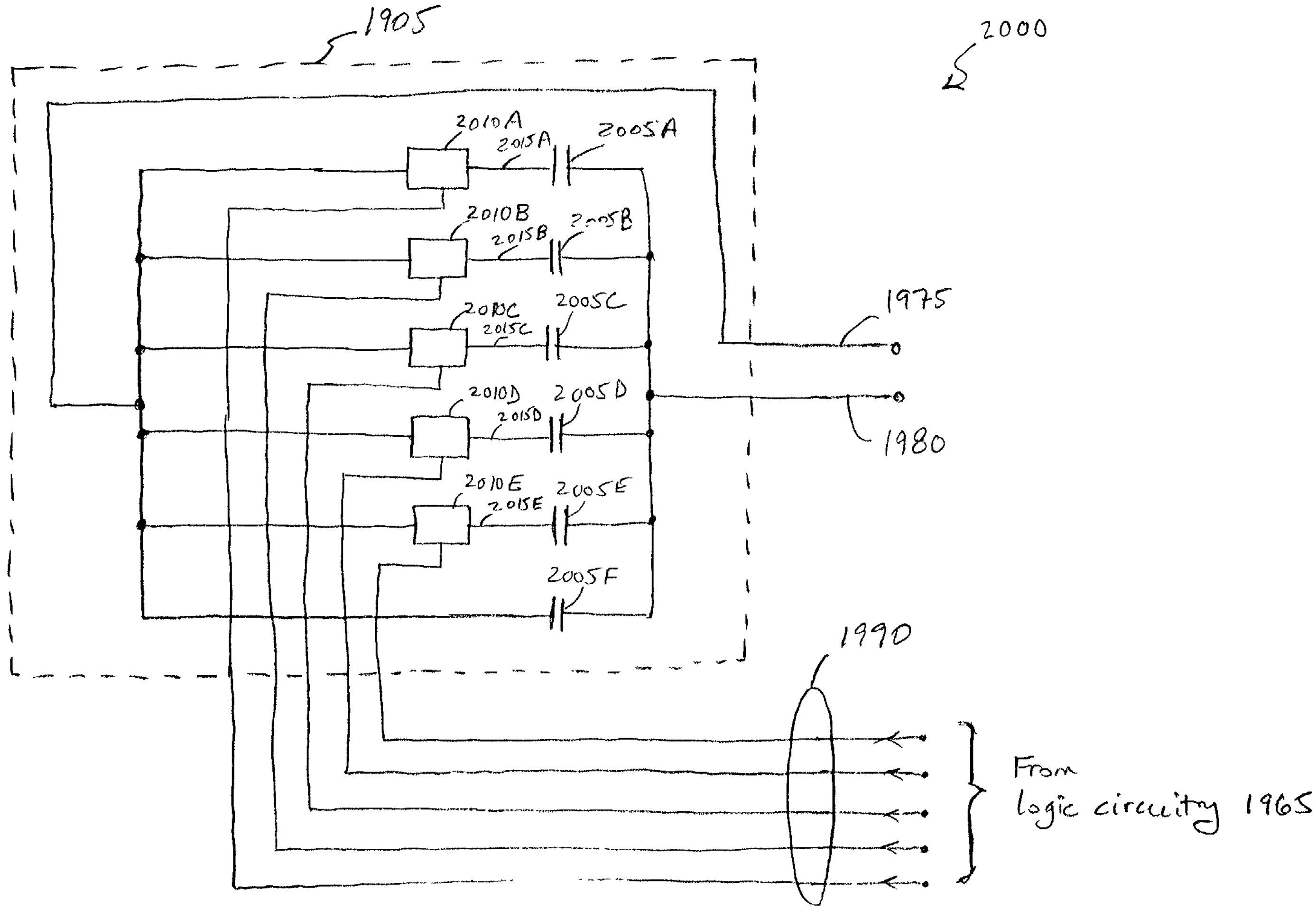

1905
2000
2010A
2015A
2005A
2010B
2015B
2005B
2010C
2015C
2005C
2010D
2015D
2005D
2010E
2015E
2005E
2005F
1975
1980
1990
From
logic circuitry 1965

FIG. 20

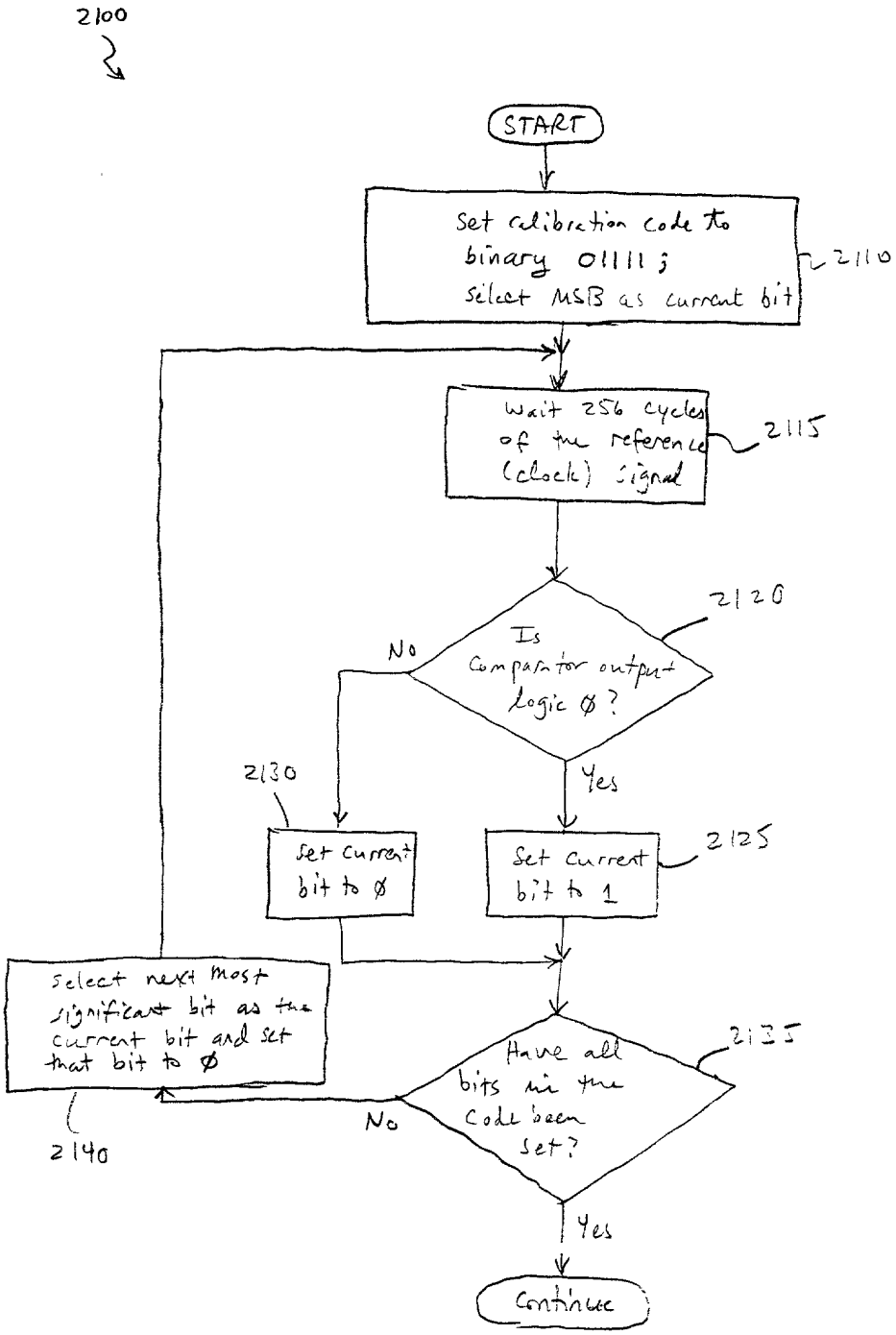

2100
START
Set calibration code to binary 01111; select MSB as current bit
2110
Wait 256 cycles of the reference (clock) signal
2115
Is Comparator output logic Ø?
2120
No
Yes
2130
Set current bit to Ø
Set current bit to 1
2125
Select next most significant bit as the current bit and set that bit to Ø
2140
Have all bits in the code been set?
2135
No
Yes
Continue

FIG. 21